Design of Digital system: 2014 Fall Final

Jan 14, 2015

Close book, 170 minutes (PM 1:10~4:00)

110 points in total

1. Implement a full adder with two 4×1 multiplexers. Note that you can use the symbol illustrated in Fig.1 for your design directly but the inputs and outputs of MUX should be defined in your answer. (15%)

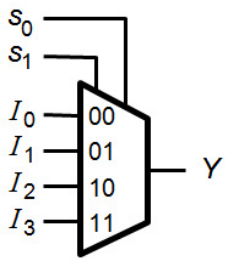

Figure 1

2. A Moore sequential network with one input *w* and one output *z* is shown in Figure 2.
   (a) Derive the corresponding state table and state diagram. (10%)
   (b) Explain the function of this finite state machine. (5%)

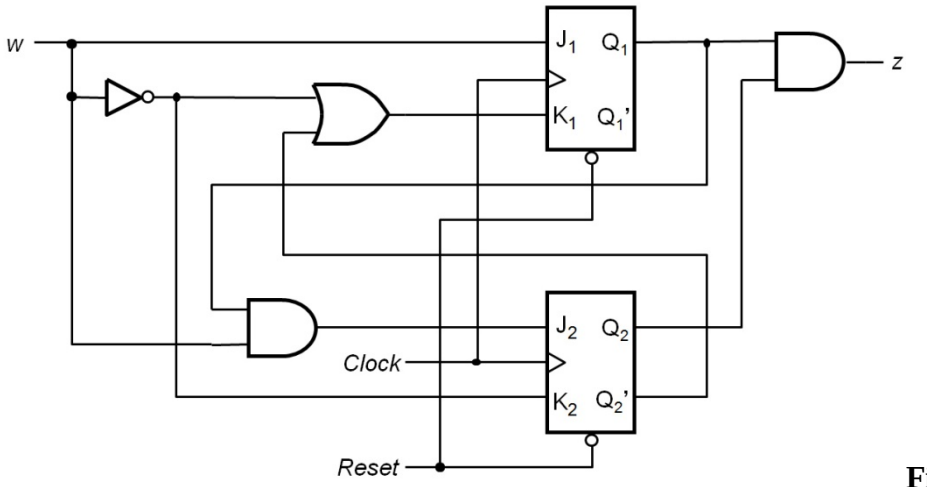

Figure 2

3. A Mealy sequential network has one input *X*, one output *Z*, and two flip-flops. A timing chart for the network follows (Fig.3). Construct a state table and state diagram for the network. (20%)

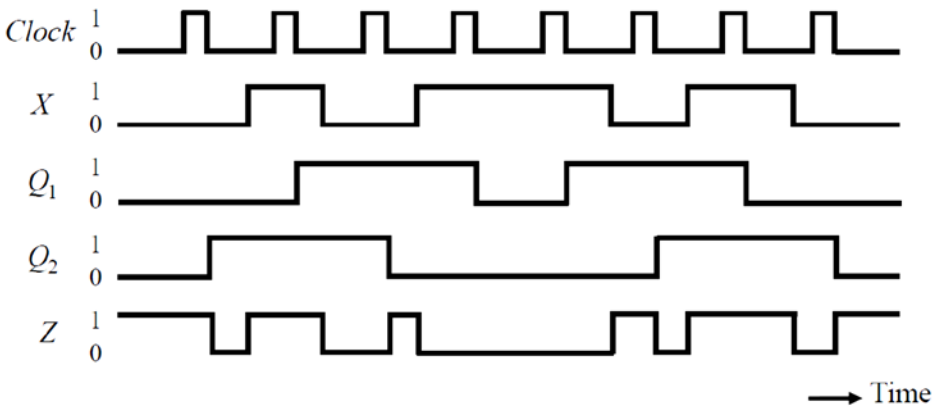

Figure 3

4. An *MN* flip-flop works as follows: (22%)
   If *MN* = 00, the next state of the flip-flop is 0.
   If *MN* = 01, the next state of the flip-flop is the same as the present state.
   If *MN* = 10, the next state of the flip-flop is the complement of the present state.
   If *MN* = 11, the next state of the flip-flop is 1.
   (a) (6%) Complete the excitation table of the *MN* flip-flop. (Use don't care when possible.)
   (b) (12%) Using the above table and Karnaugh maps, derive and minimize the input equations for a counter composed of three *MN* flip-flops which counts in the following sequence:
   ABC = 000, 001, 011, 111, 110, 100, 000 ….
   (c) (2%) Explain if your design in (b) is a self-correcting counter.

5. Design a serial 2's complementer with a right shift register and a D-type flip-flop, both of them triggered by the same clock pulse.
   (a) Plot the state diagram with clear definition of each state. (8%)
   (b) Plot the logic circuit diagram of the serial 2's complementer. You can use a block with a serial input, a serial output, and a clock input to represent the shift register. The binary number is shifted out from the side of LSB and its 2's complement is shifted into MSB of the register. (8%)

6. (a) What kind of programmable logic device (PLD) is shown in Figure 4? (4%)
   (b) Design a PROM to replace it and mark the fuse map with the cross '×' sign. (10%)

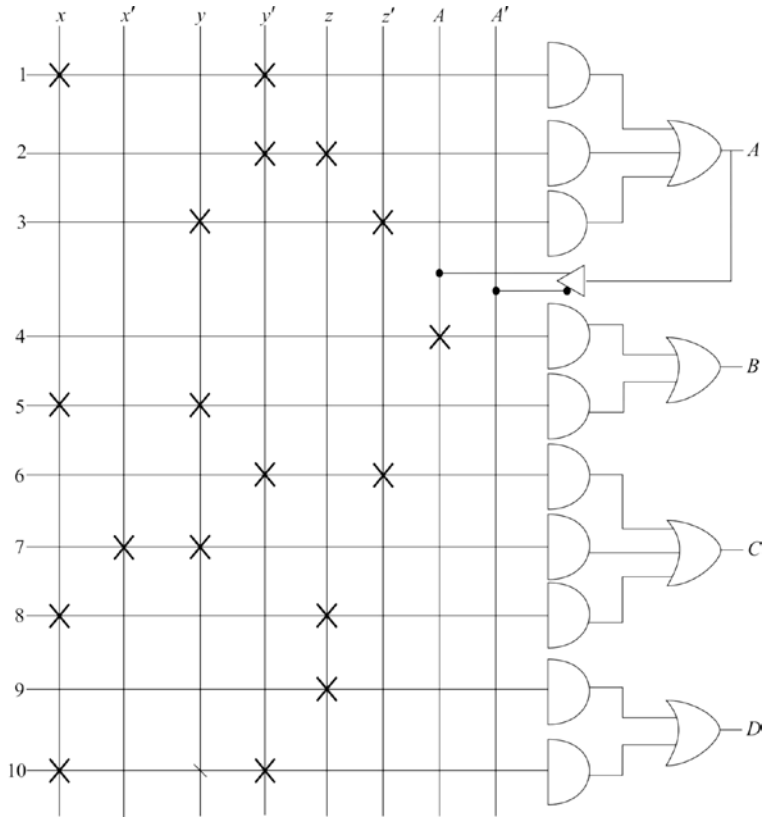

Figure 4

7. A 64K × 16 memory uses coincident decoding by splitting the internal decoder equally into *X*-selection and *Y*-selection.
   (a) What is the size of each decoder? (4%)
   (b) Determine the *X* and *Y* selection lines that are enabled when the input address is the binary equivalent of 36952. (6%)

Happy new year and enjoy your winter vacation!