Design of Digital system: 2010 spring Final

June 25, 2010

Close book, 180 minutes (PM 6:20~PM 9:20)

120 points in total

1. Figure 1 is a logic diagram of a *D*-type flip-flop, which is only triggered by the positive edge of external clock signal (*Clk*). For the rest of time, the state of its outputs *Q* and *Q'* are maintained stable.
   (a) To complete the transition of state correctly, the *D* input must be maintained for a minimum time, so-called *hold time*, right after the positive-edge triggering. How is the *hold time* estimated by the physical delay of logic gates in the circuit? Explain your answer briefly. (5%)

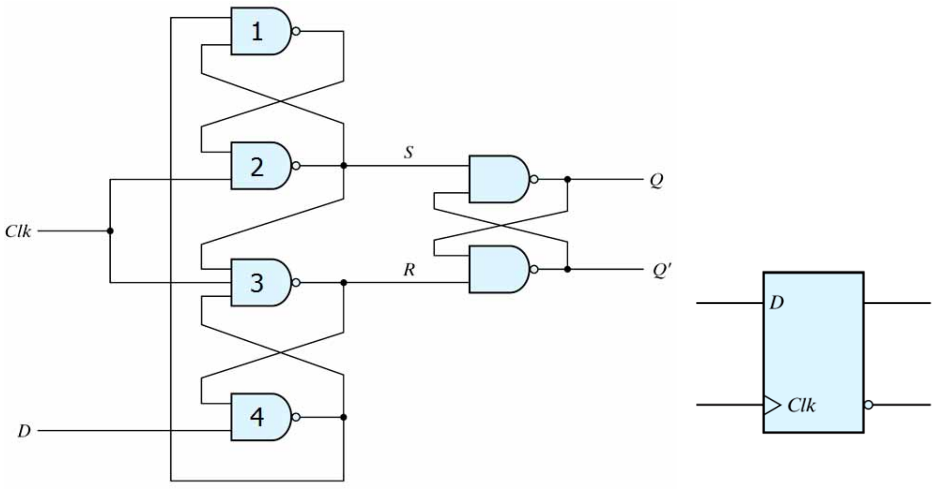

Fig.1

   (b) Construct the *T* flip-flop by using the logic block of *D* flip-flop in Fig.1. The function of asynchronous reset can be neglected here. (5%)
   (c) Design a one-input, one-output serial 2's complementer with a *T* flip-flop, which implies that only two states are enough. The circuit accepts a string of bits from the input in the order of LSB (least significant bit) to MSB (most significant bit) and generates the 2's complement at the output. For example, if the input string is 0-1-1-0-1, the corresponding output should be 0-1-0-1-0 because the 2's complement of 10110 is 01010. It can be reset asynchronously by a control bit, *reset*, which is connected to the direct reset of the *T* flip-flop to start and end the operation. (10%)

2. Consider the sequential circuit in Figure 2. It has one input signal *X* that is synchronized with the clock and one output signal *Z*.
   (a) Derive the input and output equations. (6%)
   (b) Is this a Mealy or Moore machine? Why? (4%)
   (c) Complete the state table of this circuit. (5%)
   (d) Plot the state diagram of this machine. (5%)

(e) It is known that this circuit is a sequence detector and is initialized to AB = 00 when powered up. Its output Z becomes 1 when it detects the specified sequence(s) in its input bit stream X; otherwise, Z is 0. What sequence(s) does it detect? (5%)

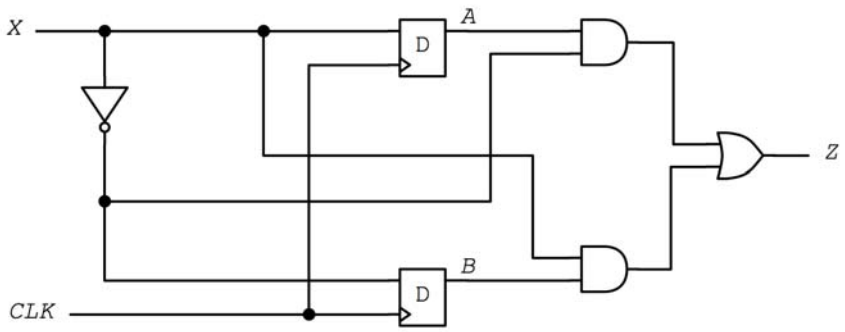

Fig.2

3. Use the four-bit binary counter with parallel load (Fig.3) to implement a mod-12 counter
   (a) with an AND gate and *Load* input. (10%)
   (b) with a NAND gate and the asynchronous *Clear* input. (10%)

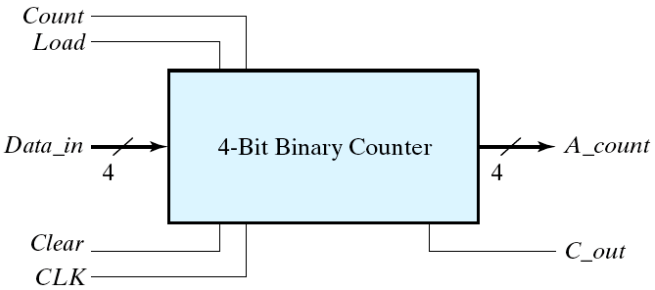

Fig.3

4. A Moore sequential network has one input and one output. When the input sequence 011 occurs, the output becomes 1 and remains 1 until the sequence 011 occurs again, in which case the output returns to 0. The output then remains 0 until 011 occurs a third time, and so forth. For example, the input sequence

   X = 0 1 0 1 1 0 1 0 1 1 0 1 0 0 1 1

   has the output

   Y = 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 1

   (a) Derive the state diagram with a maximum of six states. At this stage, each state should be assigned with an arbitrary notation, for example: an English character. In addition, you have to demonstrate that the number of state in your design has been minimized. (15%)
   (b) Obtain the minimal number of flip-flops in your design. After specifying the corresponding binary assignment of each state, complete the state table with binary numbers according to your definition. Notice that the unused states, which are treated as don't care condition, should be listed, too. (10%)

5. (a) Obtain the Hamming code word for the 11-bit data word 11001001011. (10%)
   (b) What is the original 8-bit data word that was written into the 12-bit Hamming code word 000011101010? Assume that no more than single-bit error would occur in one word. (10%)

6. Tabulate the truth table for an 8×4 ROM that implements the Boolean functions as below.

   $A(x, y, z) = \sum(0, 3, 4, 6)$

   $B(x, y, z) = \sum(0, 1, 6, 7)$

   $C(x, y, z) = \sum(1, 5)$

   $D(x, y, z) = \sum(0, 1, 4, 5, 7)$

   Please program the PROM using cross sign '×' as a temporary connection on internal logic diagram. (10%)

   Hint: An internal logic of 32×8 programmable ROM was shown in the following. Modify it to match your need.

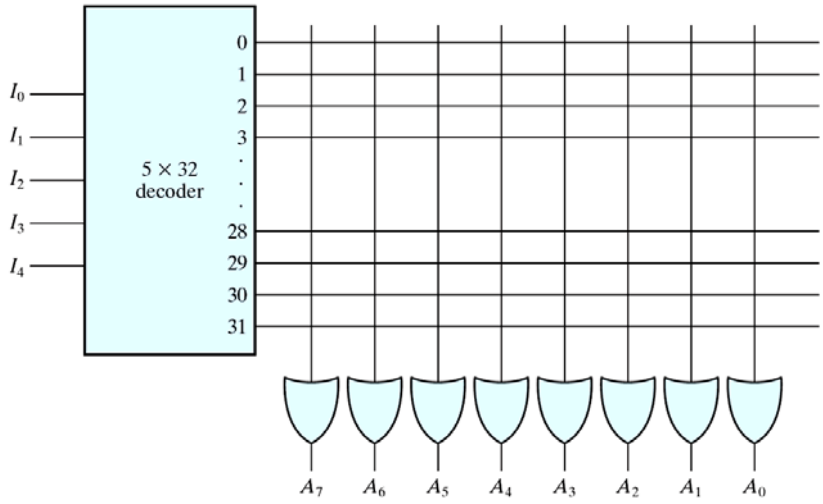

Fig.4

Don't forget our office hour for final exam: **6/30 PM 3:00~5:00** @F7016b.
Enjoy your summer vacation!