# Design of Digital system: 2014 Fall Midterm

Nov 19, 2014

Close book, 170 minutes (PM 1:10~PM 4:00)
Prime and unprimed inputs are available for all logic gate design.

1. (12%) Perform the following arithmetic operations with eight-bit 2's complement numbers and indicate whether overflow occurs. Check your answers by converting to decimal numbers.
   (a) 01110101＋11011110
   (b) 01110101－11011110

2. (a) Convert the decimal number 14959 into a hexadecimal number. (5%)
   (b) Convert the decimal fraction 0.824 into binary representation. Eight binary digits are sufficient to meet the accuracy here. (5%)

3. (a) Express the following function in sum-of-minterms and sum-of-products forms. (8%)
   $(ad + b'c + bd')(b + d)$
   (b) Express the following function in sum-of-maxterms and product-of-sums forms. (8%)
   $ad + bcd + ab'c' + b'c'd'$

4. (12%) Given AB = 0 and A + B = 1, use algebraic manipulation (i.e. K-map method is not applicable in this question) to prove that
   (A + C)(A' + B)(B + C) = BC

5. A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (*a*, *b*, *c*, *d*, *e*, *f*, *g*) select the corresponding segments in the display (a) and the logic 1 indicates a light segment. The numeric display chosen to represent the decimal digit is also shown in (b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. Note that the six invalid combinations should result in a blank display, and the logic diagram should be provided in your answer. (18%)


(a) Segment designation (b) Numerical designation for display

(a) Draw the OR-AND logic diagram to implement *b*.
(b) Draw the NAND-NAND logic diagram to implement *d*.
(c) Draw the NAND-AND logic diagram to implement *g*.

6. Design a four-input priority encoder with inputs $D_0$ through $D_3$, with input $D_0$ having the highest priority and input $D_3$ having the lowest priority. The binary code of the input (i.e., the subscript number) that has a value of logic 1 and holds the highest priority would be generated as the output bit(s). In addition to the output codes, a valid bit indicator ($V$) is also provided by this encoder and equals to 0, indicating the invalid condition, only when all inputs are logic 0. (16%)
   (a) Plot the truth table of this priority encoder. Note that the invalid input is considered don't care condition.
   (b) Obtain the output(s) in standard form.