How to design a clocked sequential ckt?

1° Define the input/output and states of the circuit.

2° Check if state reduction is necessary

3° State assignment (# of FFs)

4° Binary-coded state diagram and state table.

5° Choose the type of FFs.

6° Obtain the simplified input, output, and state equations

7° Draw the logic diagram.

Problem: Detect a sequence of 3+ consecutive logic **1**

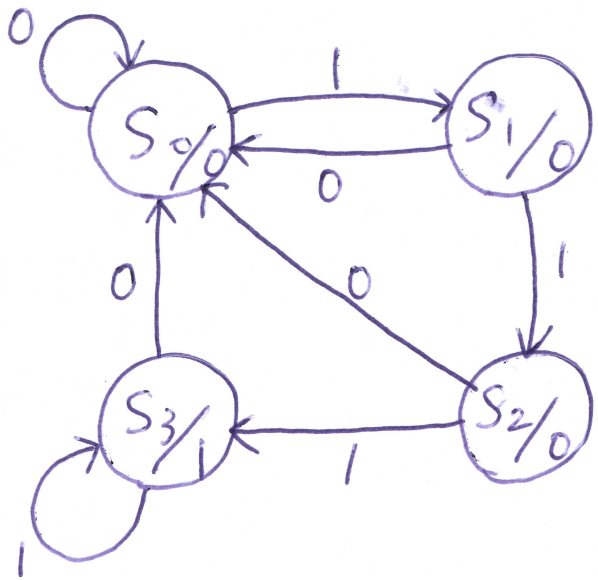
Input : x , Output = y

S_0 : 0 is received (y=0)

S_1 : 01 is received (y=0)

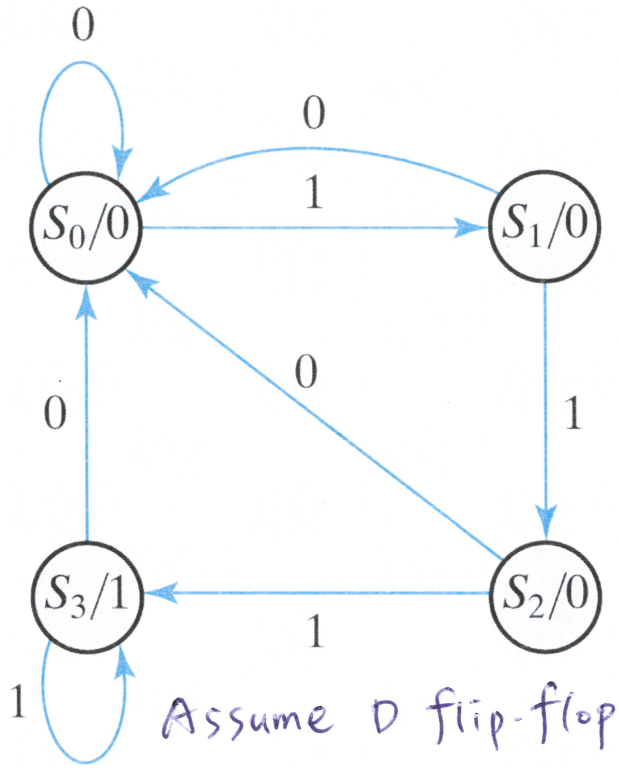
S_2 : 011 is received (y=0)

S_3 : 111 is received (y=1)



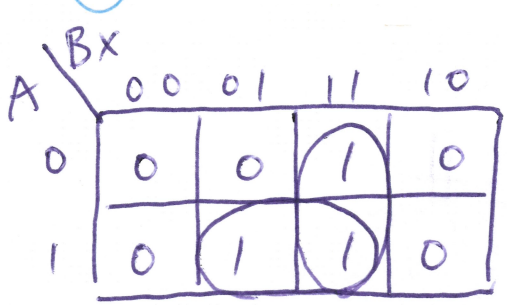
Let A and B indicate states S_0 to S_3

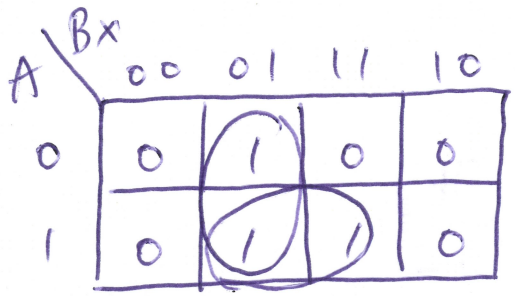
	A	B
S_0	0	0
S_1	0	1
S_2	1	0
S_3	1	1

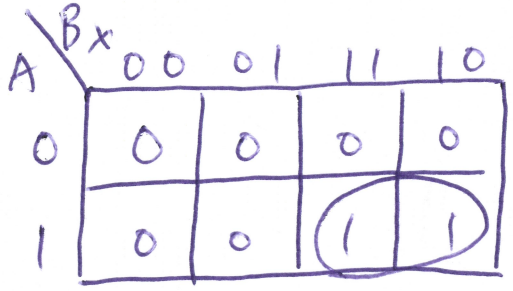


Present States A	B	Input x	Next States A(t+1)	B(t+1)	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Assume D flip-flops are used for implementation.



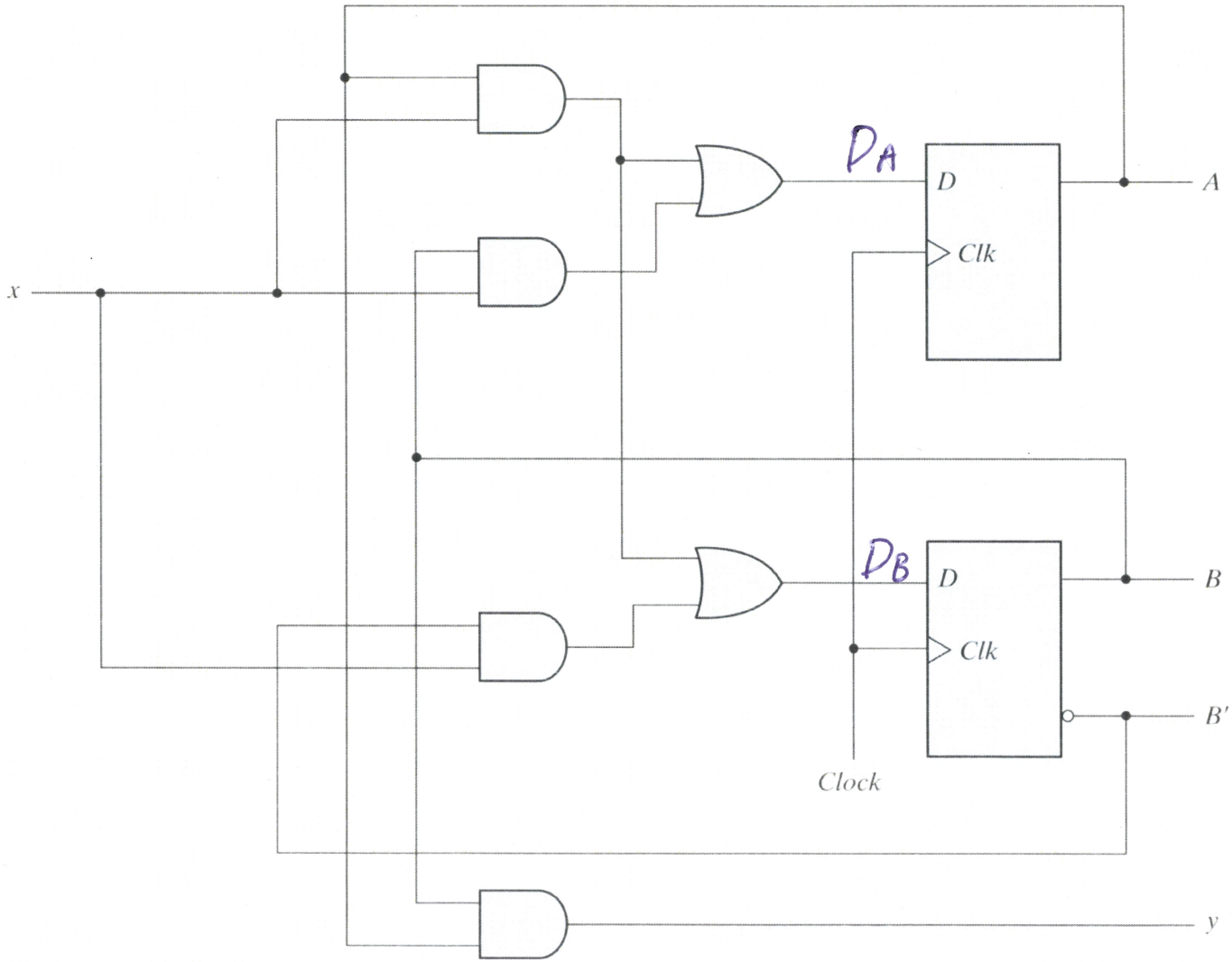




$A(t+1) = Ax + Bx = D_A$ $\quad B(t+1) = Ax + B'x = D_B$ (State / Input Eq.)

$y = AB$ (Output Eq)

Sequence detector with D flip-flops



Synthesis using JK or T flip-flops?

Given state equation $Q(t+1)$, how to obtain the corresponding input equation of JK or T flip-flop?

For JK FF, $Q(t+1) = \boxed{J}Q' + \boxed{K}Q$

For T FF, $Q(t+1) = T \oplus Q$

⇒ Excitation table

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Synthesis using "JK" flip-flops

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

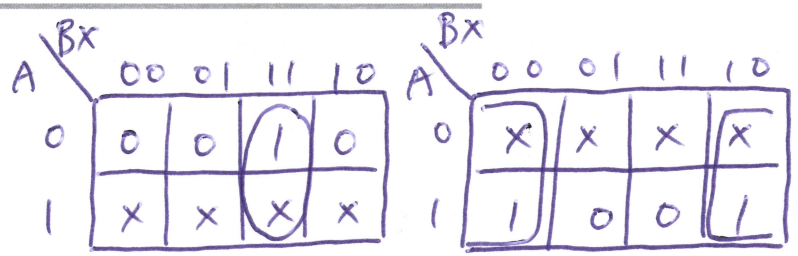
Table 5.11
State Table for Sequence Detector

Present State		Input	Next State		Output				
A	**B**	**x**	**A**	**B**	**y**	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	0	0	0	X	X	1
0	1	1	1	0	0	1	X	X	1
1	0	0	0	0	0	X	1	0	X
1	0	1	1	1	0	X	0	1	X
1	1	0	0	0	1	X	1	X	1
1	1	1	1	1	1	X	0	X	0

$A(t+1) = xA + xB$

$B(t+1) = xA + xB'$

$Q(t+1) = JQ' + K'Q$



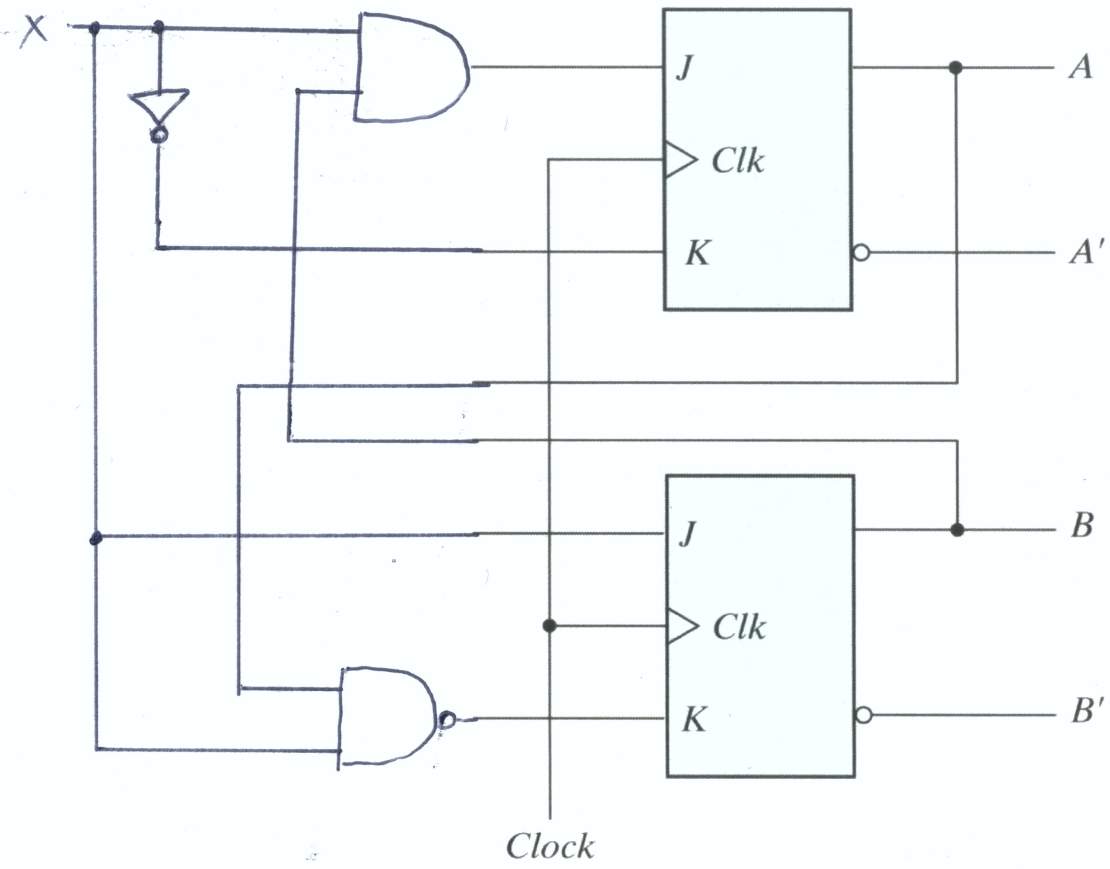
$J_A = Bx$

$K_A = x'$

$J_B = x$

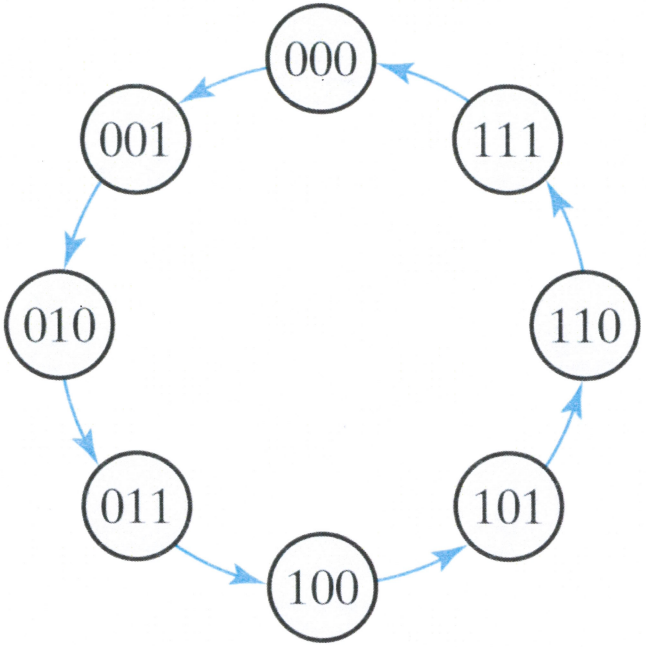
$K_B = A' + x'$

Synthesis using JK flip-flops



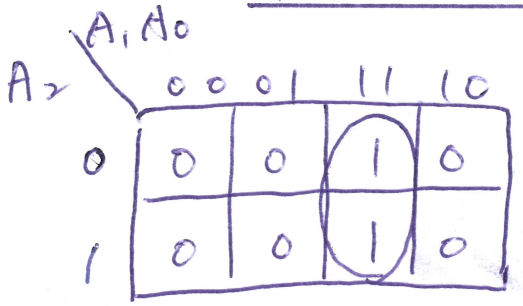
$K_B = A' + x' = (Ax)'$

Problem: Design a 3-bit binary counter with T flip-flops

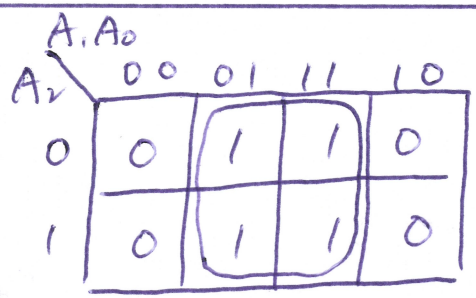


No input, no output, 3 FFs.

Present States			Next States					
A_2	A_1	A_0	A_2	A_1	A_0	T_{A_2}	T_{A_1}	T_{A_0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



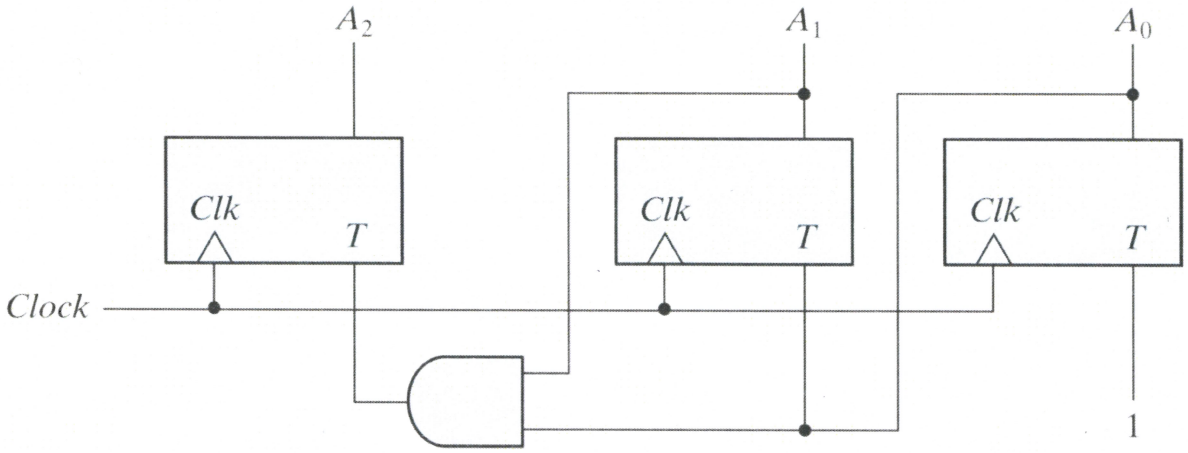
$T_{A_2} = A_1 A_0$



$T_{A_1} = A_0$

$T_{A_0} = 1$

Synthesis using T flip-flops



A_1 will change only when $A_0 = 1 \Rightarrow T_{A_1} = A_0$

A_2 will change only when $A_1 = A_0 = 1 \Rightarrow T_{A_2} = A_0 A_1$