Design of Digital System: Fall 2017

Time and Location:
(甲班) Wednesday AM 9:10~12:00 @ EC3012

Instructor:
莊子肇, Associate Prof.
Office: EC8006, Dept. of Electrical Engineering
Phone: 07-525-2000 ext. 4196
Email: chuang@mail.ee.nsysu.edu.tw
Office Hour: Tue/Wed PM 2-4 (by appointment)

Website: (Class notes and news are released here.)
http://bmilab.ee.nsysu.edu.tw/lab/course_digital.html
Facebook 社團：「數位系統設計：中山電一甲 2017」

Textbooks/References:
滄海圖書公司代理 04-2708-8787

Schedule:
Week 1, 2 Digital system and binary numbers
Week 3, 4 Boolean algebra and logic gates
Week 5, 6 Gate-level minimization
Week 7, 8 Combinational logic
Week 9 Midterm
Week 10-12 Synchronous sequential logic
Week 13, 14 Registers and counters
Week 15, 16 Memory and programmable logic
Week 17 Design at the register transfer level
Week 18 Final

Grading:
Homework/Quiz 40%
Midterm 35%
Final 35%