Design of Digital System: Fall 2018

Time and Location:
(甲班) Wednesday PM 1:10~4:00 @ EC2007

Instructor:
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Website: (Class notes and news are released here.)
http://bmilab.ee.nsysu.edu.tw/lab/course_digital.html
Facebook 社團：「數位系統設計：中山電一甲 2018」

Textbooks/References:
滄海圖書公司代理 04-2708-8787

Schedule:
Week 1, 2  Digital system and binary numbers
Week 3, 4  Boolean algebra and logic gates
Week 5, 6  Gate-level minimization
Week 7, 8  Combinational logic
Week 9  Midterm
Week 10-12  Synchronous sequential logic
Week 13, 14  Registers and counters
Week 15, 16  Memory and programmable logic
Week 17  Design at the register transfer level
Week 18  Final

Grading:
Homework/Quiz  40%
Midterm  35%
Final  35%